FAULT PROCESSING SYSTEM OF TRANSFER DEVICE

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Abstract of **JP61046543**

PURPOSE:To reduce the overhead of a CPU by resetting a transfer device CH or I/O when a service processor (SVP) logs out fault information on the CH, and then sending out the result to a transfer controller (CHP). CONSTITUTION:If a fault occurs to a transfer device CH31, the SVP4 is interrupted through an interruption line I2. The SVP4 logs out fault information through an interface bus IB2 and files it, and then recognizes the fault contents. The SVP sends a clear instruction to the CH31 when the fault is a machine check error or to the I/O5 when an interface check error. The result of this clearing operation is read through the bus IB2 to generate status information corresponding to the result, and the information is sent out to a CHP3 through the bus IB2. The CHP3 sets the status information in a specific area of a channel status word and initiates a normal end interruption to the CPU2.